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EXAMINER
ROSS, JOHN M

ART UNIT	PAPER NUMBER
2188	3

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

●	Application N ● 10/086,494	Applicant(s) SOLTIS, DONALD CHARLES
Office Action Summary	Examiner John M Ross	Art Unit 2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _01 March 2002_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-26_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-26_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _01 March 2002_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

    a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _3_.

4)☐ Interview Summary (PTO-413) Paper No(s). _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1.   The Information Disclosure Statement(s) received 01 March 2002 has been considered.

Please see attached PTO-1449(s).

Drawings

2.   The drawings filed on 01 March 2002 have been approved by the Examiner.

Claim Objections

3.   Claims 2 and 10 are objected to because of the following informalities:

Claims 2 and 10 appear to be missing a conjunction and a verb. It is suggested that the word "and" be inserted before the phrase "the crossbar", and the word "is" be inserted before the word "configured" in line 2 of both claims.

Appropriate correction of the above noted deficiencies is required.

Claim Rejections - 35 USC § 112

4.   The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5.   Claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The claim recites that the crossbar is configured to synchronize asynchronous transactions between a processor and a cache, however the specification merely states this feature and does not give an adequate description to support this limitation (Page 6, paragraph 24; page 11, paragraph 35).

To one of ordinary skill in the art, it would not be readily apparent how the crossbar could be configured in order to synchronize transactions without modification, because a crossbar switch does not inherently provide synchronization and there is nothing in the specification to indicate how this function is provided. Furthermore, it is not clear from the specification what the asynchronous nature of the problem entails, so that one of ordinary skill would not be able to make or use the invention as set forth in the claim.

Accordingly, prior art has not been applied to claim 18.

Claim Rejections - 35 USC § 102

6.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7.   Claims 1-4, 6, 12-15, 20-21, 23-24 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli (US 6,532,519).

As in claims 1-4, 6 and 12-13, Arimilli discloses a system including a processor (Fig. 1, element 11a), a main memory (Fig. 1, element 18), a cache (Fig. 1, element 14a), and an interface between the processor and the cache (Fig. 1, element 20), where the cache is configured to receive data from an address of the main memory upon a request for the data by the processor (Column 1, lines 30-34), and the interface may be a crossbar (Column 2, lines 17-19).

As in claim 2, Arimilli discloses the above system wherein the main memory is controlled by a memory controller (Fig. 1, element 17), and the crossbar interface is configured to link the memory controller, the processor and the cache (Fig. 1, element 20; column 2, lines 17-34).

As in claim 3, it is inherent in the teachings of Arimilli that when the processors and cache are connected by a crossbar switch as in claim 1 above, the connections to the crossbar are made through a plurality of ports (Fig. 1). Also as in claim 3 Arimilli teaches that a single address space may be partitioned among two or more caches such that a link between the

processor and cache would be made based upon the main memory address of a request for data

by the processor (Column 1, lines 30-34; column 3, lines 51-67).

As in claim 4, Arimilli teaches that the processor is configured to associate a main

memory address range (i.e. address space) with the cache (Column 1, lines 30-34; column 3,

lines 51-67).

As in claim 6, Arimilli teaches that a main memory address range is mapped to the cache

(Column 1, lines 30-34; column 3, lines 51-67).

It is noted in the rejections of claims 3-4 and 6 that mapping a main memory address

range to a cache, and storing and retrieving data in the cache based upon a main memory address

contained in a request from a processor, are well-known fundamental properties of any cache

memory system such as that disclosed by Arimilli.

As in claim 12, it is axiomatic in the system of Arimilli that the crossbar interface

comprises at least one crossbar (Column 2, lines 17-19).

As in claim 13, the system of Arimilli comprises a plurality of processors linked with the

cache via the crossbar interface (Fig. 1, elements 11a – 11e; column 2, lines 17-24).

As in claims 14-15, Arimilli discloses a system comprising a plurality of processors (Fig.

1, elements 11a – 11e), a main memory (Fig. 1, element 18), a plurality of caches (Fig. 1,

elements 14a – 14e), and an interface linking the caches and the processors (Fig. 1, element 20),

where the cache is configured to receive data from a range of the main memory upon a request

for the data by one of the processors (Column 1, lines 30-34), and the interface may be a crossbar

(Column 2, lines 17-19).

As in claim 15, Arimilli discloses that the processors may be configured to share at least

one of the caches via the crossbar interface (Column 2, lines 38-43).

As in claim 20, Arimilli discloses a system configuration where

a plurality of main memory address ranges is mapped to a plurality of caches (Fig. 1,

elements 14a – 14e and 18; column 1, lines 30-34; column 3, lines 51-67);

the caches are mapped to a plurality of processors (Fig. 1, elements 11a – 11e; column 2,

lines 38-43); and

the processors and caches are linked using a crossbar interface (Fig. 1, element 20;

column 2, lines 17-19).

As in claim 21, Arimilli discloses that a processor is configured to interface with a cache

(Column 2, lines 38-43), where also it is noted that mapping a main memory address range

addressable by a processor to a cache is a well-known fundamental property of any cache

memory system such as that disclosed by Arimilli.

As in claim 23, Arimilli discloses that a cache may be mapped to more than one

processor (Column 2, lines 38-43).

As in claim 24, Arimilli discloses that two or more caches may be merged to act as a

single larger cache (i.e. change the size of a cache) and that this association only requires

programming a mode register and therefore does not require changing the crossbar interface

(Column 2, line 49 to column 3, line 5; column 3, lines 44-67).

As in claim 26, Arimilli teaches that more than one cache may be mapped to one

processor (Column 3, lines 51-58).

Claim Rejections - 35 USC § 103

8.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

9.   Claims 5, 7-10, 16-17 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Arimilli (US 6,532,519) as applied to claims 1, 4, 14 and 20 above, and further in view of

Hassoun (5,737,757).

Arimilli is relied upon for the teachings relative to claims 1, 4, 14 and 20 as above.

The rationale derived from Arimilli in the rejection of claim 13 above is incorporated herein for the teaching that a plurality of processors is linked with the cache via the crossbar interface as in claims 7-10.

The rationale derived from Arimilli in the rejection of claim 3 above is incorporated herein for the teaching that a single address space may be partitioned among two or more caches, and that the crossbar interface comprises a plurality of ports via which a cache and a processor are linked based on the main memory address as in claim 10.

Arimilli does not teach that the processor is linked with the cache based on an address range stored in the processor corresponding to a range of addresses in the main memory mapped to the cache as required by claim 5.

Arimilli also does not teach that the processor comprises an address range table wherein each address range is associated with a cache as required by claim 7, and where the table is programmable as required by claim 8.

Arimilli also does not teach that the processor comprises a plurality of address ranges and module identifiers corresponding to the caches as required by claims 9-10.

Arimilli also does not teach that a cache and processor are linked based on a module identifier supplied by the processor as required by claims 16-17.

Arimilli also does not teach that module identifier is associated with a main memory address range in a processor as required by claim 22.

Hassoun teaches a plurality of processors linked to a plurality of memories through a crossbar interface, where the address space of the memory is partitioned into separate address ranges (Fig. 1; column 2, lines 3-5; column 4, lines 20-25). Hassoun further teaches that a transaction initiated by a processor for accessing the memory contains a module identifier of the memory module to which the transaction is sent (Column 4, lines 26-39; column 5, lines 54-63).

It is readily apparent in the foregoing teachings of Hassoun that in order to send the proper identifier of the module associated with the memory address referenced in the transaction, so that the crossbar can direct the transaction to the proper module, the processor must store information to associate the address range mapped to each memory module with the module identifier (i.e. a table).

Regarding claims 5, 7, 9-10, 16-17 and 22, it would have been obvious to one of ordinary skill in the art at the time of invention by applicant to apply the teachings of Hassoun regarding directing transactions between a processor and a main memory over a crossbar interface, to the problem of directing transactions between a processor and a cache memory over a crossbar interface in the system of Arimilli, noting that it is well known to interface a cache memory to a processor in place of a main memory in a manner that is transparent to the processor, in order to improve memory access time. Therefore, it would likewise have been obvious to link a

processor with a cache based on a main memory address range corresponding to a range of

addresses mapped to the cache, where the address range is stored in an address range table in the

processor containing a plurality of address ranges such that each address range is associated with

a cache, and where each cache is identified by a module identifier, as taught by Hassoun, in the

system of Arimilli, in order to direct memory transactions to the proper receiving module as

taught by Hassoun.

Regarding claim 8, it would have been obvious to one of ordinary skill in the art at the

time of invention by applicant to make the address range table programmable because it is well

known in the art to make configuration data in a system programmable in order to flexibly adapt

the system to changing conditions such as the addition, deletion, or failure of components in the

system.

10.   Claims 11 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli

(US 6,532,519) as applied to claim 1 above, and further in view of Handy (Jim Handy, The

Cache Memory Book, 1998).

Arimilli is relied upon for the teachings relative to claims 1 and 14 as above.

Arimilli does not teach that the system is configured to deliver data from the memory to

the cache and the processor at the same time as required by claims 11 and 19.

Handy teaches a cache memory system where upon a read miss, the cache and the

requesting processor receive data delivered from a main memory simultaneously so that the new

data is available from the cache in the event of a subsequent access to the same data (Page 46,

Fig. 2.4b; pages 44-45, paragraph 4).

It would have been obvious to one of ordinary skill in the art at the time of invention by

applicant to deliver data from the memory to the cache and the requesting processor

simultaneously as taught by Handy, in the system of Arimilli, so that the new data would be

available from the cache in the event of a subsequent access to the same data as taught by Handy.

11.   Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (US

6,532,519).

Arimilli is relied upon for the teachings relative to claim 20 as above.

Arimilli does not teach that the system is configured on a single die as required by claim

25. However, it is well known in the art that fabricating multiple components on the same die

can improve speed and reduce power consumption.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of

invention by applicant to configure the processing system of Arimilli on a single die in order to
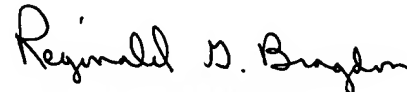
improve speed and reduce power consumption.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M Ross whose telephone number is (703) 305-0706. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

JMR

REGINALD G. BRAGDON
PRIMARY EXAMINER